Procedure for Testing MuTr CPA chips:

The MuTr CPA chips are very sensitive to static and moisture. Desiccant silica gel and a humidity indicator are kept with the chips in their storage bags. Anti-static precautions must include, but are not limited to, use of a grounded, anti-static mat or other surface on which chip testing will be performed and a grounded, anti-static bracelet. The grounding of theses items should be to the third-wire ground of an electrical outlet.

The software used to control the chip testing board and the external pulser is Labview run from a PC. (This is entitled the Automated Muon Pre-Amp ASIC Test.) Open the program found on the desktop entitled, "testing.vi". This should take a few moments to start up because it is initializing the other devices.

Open a box and carefully take out the silver bag containing trays of chips. These trays are interlocking and must be removed together. Each chip has an assigned compartment in a tray. Numbering goes from the right to the left. Avoid touching the chips. To pick up a chip, use a "pen-vac," a suction device that resembles a pen. Press the button of the pen- vac and place firmly on the label of a chip. Release the button to create suction between the pen and the chip. To brake the suction, press the button a second time. A more reliable electrical, vacuum pump can be used when available. Take care when moving the chips because their pins are easily bent.

The test stand clamp, or clamshell, is the large black case near the front of the board. It is opened by a release mechanism on the front of the clamp. Place a chip in the clamp with the chip's notch, a small indentation on the top surface of each chip, pointing toward the ground terminal from the cable from the external pulser. Close the clamp lid.

With a chip clamped in the test board, the power supplies should be turned on in this order: +/-5V Digital, +/-5V Analog, and +/-15V Analog. Check the current on the +/-5V Analog Power supply. The proper current is around 1.73 A. If the current is lower than 1.63 A or higher than 1.83 A, the chip is bad and no further testing is necessary. The voltage settings with the nominal current readings are:
Digital Power settings: 8 to 8.4V, 0.7amps
+/-5V Analog Power settings: 6.4V, 1.74amps -6.4V, 0.47amps
+/-15V Analog Power settings: 10V, 0.29amps -10V, 0.18amps
The current readings may deviate by +/- 10% and may change once testing has started.

Input the file name in which the test results will be stored, including the path, in the appropriate box in the "testing.vi" window. Usually the file name is the chip id number preceded by a directory for the chip's box, omitting the "c:\", for example: "box2\m1900\cpa1901." The path must be identical to an existing folder in the C drive. Without the chip id, the program will not function. The file folders in which the test results are stored can hold files for only 15 to 20 chips due to an MS operating system limitation.

Toggling the “on” switch on the “testing.vi” window starts the testing process for a chip. The program does not need to be restarted between tests. The program always fails the first test it performs after initialization. This bug has never been worked out. Simply retest the chip. The program runs five tests on each chip. The chips will fail if they lie outside designated windows for pedestal height and shape (deviation), pulse height and width. Chip response can improve with repeated testing so failing chips should be retested. Exceptions to this are chips are chips that draw too much or too little current (see above) and chips with one or more unresponsive channels.

When the five tests have been run for a chip, the program will return an overall pass or fail for the chip. Turn off the power in the reverse order they were turned on: +/-15V Analog, +/-5V Analog, +/-5V Digital. Remove the chip from the test board using the suction device. Return it to the tray. If the chip is bad, mark the top of the chip with a red dot or an “X” and record the failure in the logbook. Proceed to the next chip. Make sure to enter the new chip id so that saved data correlates to the proper chip.

Many times, the FPGA does not function properly and the pulse arrives too late to be detected. The test will fail when this happens. It is necessary to consider this, especially if there is no pulse visible in the pulse histogram of tests 2, 3, 4, or 5.

Setup:

Necessary supplies:
2 10V power supplies
3 5V power supplies
1 test stand
1 PC with proper card to connect to cables
2-3 power strips
1 pulse generator
1 PHENIX MUON Cathode Pre-amp ASIC Tester/Pulser
1 circuit to pick up signals for pulsing in a BNC box

The test board has been mounted in an aluminum box with labels. As seen in the following diagrams, there are few connections to be made. The first diagram shows the connections made to the board. Connections are made to the power supplies as seen in the second diagram.

The CAMAC Control and CAMAC Power can be disregarded for the testing process.

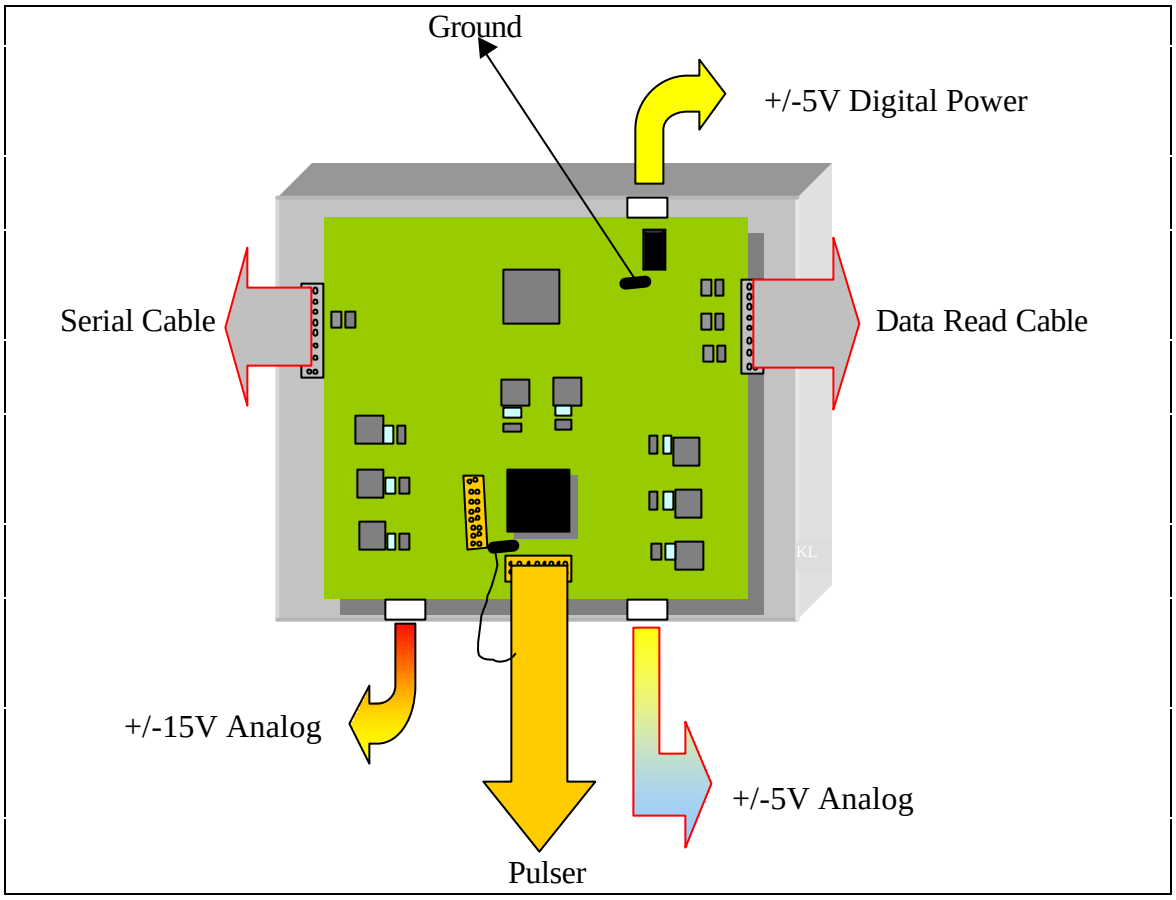
The serial cable is marked with tape and it’s connector on the board is labeled. The same is true for the data read cable. These cables are connected at the other end which goes into the back of the computer. It fits into a slot near the base of the tower. Data read is the top part of the cable.

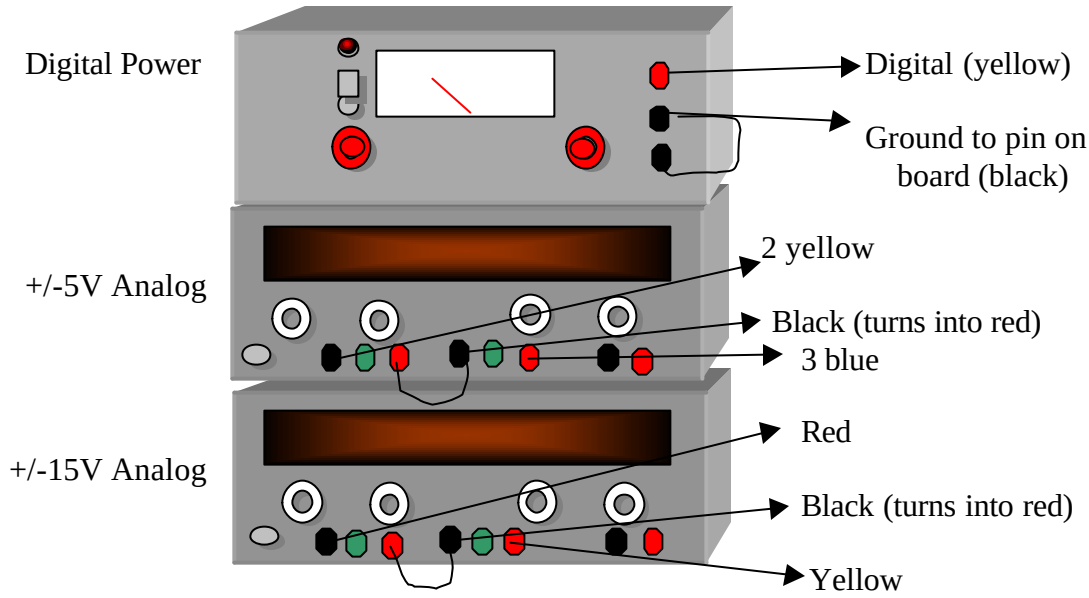
Digital power is connected via a single yellow wire. A ground must be connected to a nearby pin (see diagram). The top power supply in the diagram is designated to be digital. The single yellow wire is joined to the positive terminal on the supply. A jumper is run between the negative terminal and ground which are connected to a point on the board near the digital power input as seen in the diagram.

+/-5V Analog power is connected via a cable made up of 1 red wire, 2 yellow, and 3 blue. In the diagram, the middle power supply is +/-5V Analog. The double yellow wires are connected to the negative terminal. The positive return is grounded and connected the black wire (which turns into a red one.) The three blue wires are connected to the positive terminal.

+/-15V Analog power, the bottom power supply in the diagram, has a cable with 2 red wires and 1 yellow. The terminal connection on the board is labeled positive, negative, and ground to correspond to the power supply terminals. Again, the return terminals are connected to ground.

A copper colored cable connects the pulser to the board on a socket that sticks up out of the board. Press the connector firmly down and then connect the wire that sticks out on the top of the cable to the silver globular mass directly to the left of the clamshell. The pulser is connected to the output of the pulse generator. Input into the pulse generator is the connection from the BNC box with according circuitry. The box is connected to four pins. Ground is pin 50 on the JP18 connector. The enable switch is connected to pin 21 on the JP20 connector. +5V of power is picked up near the digital power; it is the middle of three pins. Finally, the reset from the test stand is picked up on the right side of the stand on the connector JP18, pin 14.


Ground
+/-5V Digital Power
Serial Cable
Data Read Cable
+/-15V Analog
+/-5V Analog
Pulser


Digital Power
Digital (yellow)
Ground to pin on board (black)
+/-5V Analog
2 yellow
Black (turns into red)
3 blue
+/-15V Analog
Red
Black (turns into red)
Yellow